REMARKS

The above Amendments and these Remarks are in reply to the Office Action mailed May 11, 2005.

Currently, claims 1-36 are pending. Applicants respectfully request reconsideration of claims 1-36

I. Summary of the Examiner's Objections

Claims 1-3, 5-17, 19, 20 and 25-36 were rejected under 35 USC 102(b) as being anticipated by *Etoh et al.* (USP RE37593).

Claims 4 and 18 were rejected under 35 USC 103(a) as being unpatentable over *Etoh et al.* (USP RE37593) in view of *Hellums* (5,362,988) (previously cited).

Claims 21-24 were rejected under 35 U.S.C. 103(a) as being unpatentable over *Etoh et al.* (USP RE37593).

II. Summary of the Amendments

No claims are amended.

III. Remarks

It is respectfully submitted the claims are not anticipated by nor obvious in view of *Etoh et al.*

Each of the claims calls for "a bypass enable signal operable *responsive to a signal generated by the host device indicating that the power up of the host is complete*" (Claim 1 emphasis added) or a method "responsive to a power up completion signal from a host device," (Claim 16). No such signal is disclosed or taught by *Etoh et al.*

In particular, it will be shown that:

- Element 2 of *Etoh et al.*, cited as a "host device", is not a "host device" as such limitation is used in the claims. Element 2 is a power supply which retrieves an external voltage. Even if element 2 were a "host device", it does not provide a control path and a "host voltage" – there is only one signal from element 2. By definition then, there is no "bypass enable" which is responsive from element (2).

- Whether or not element 2 is considered a host device, the invention is not anticipated because the alleged bypass enable signal (LM) is not responsive to a signal generated by the host device indicating that power up is complete. The LM signal is responsive only to the level of the "host voltage"; there is no separate control signal and host voltage.
- The signal which the bypass enable is alleged to be responsive to - signal (4) - does not communicate with the bypass, and does not communicate anything indicating that the host power up is complete.

Claim 1-3, 4 – 15

Claim 1 calls for:

> A memory system including *a control path to a host device*, the host device supplying *a host voltage*, comprising:
>
> ...
>
> a bypass enable signal operable *responsive to a signal generated by the host device indicating that the power up of the host is complete. (emphasis added)*

Initially, it is noted that the "host voltage" and the "signal generated by the host device indicating that the power up of the host is complete" are separate elements of the claim.

As understood, the Examiner identifies the "host device" as element 2 of *Etoh et al.* However, as noted in the specification of *Etoh et al:*

> Numeral 2 is an exemplary power supply circuit which detects a drop of an external power supply voltage (Vext) to shift the LSI chip into a back-up state by a battery. This power supply circuit serves to prevent data stored in the LSI chip from disappearing even when Vext is lowered due to shut-down of the commercially available power source. (Col 4., lines 59 – 65)

This power supply circuit is not a "host device" within the meaning of such term as defined in the claim. The power supply circuit detects a drop in an "external power supply voltage" i.e. a host voltage. If the Examiner maintains that element (2) of *Etoh et al.* is a host device, then no "control path" to the device from the memory system (clearly element 5 of *Etoh et al.*) exists. The only connections between element 2 and element 1 are a supply or "host voltage". Hence, claim 1 is not anticipated.

Irrespective of whether element 2 is considered a "host device", there is no "bypass enable" signal as defined in the present claims. Moreover, the Examiner indicates that the bypass element is

element SWa. Indeed, as noted in *Etoh et al.:*

> SW6a and SW6c are a switch for directly apply the power supply voltage Vcc to the circuit blocks when Vcc is decreased to a value substantially equal to V_{CL1} or V_{CLW}. (wol 6, lines 5 – 8)

However, SWa and SWc are controlled by a signal LM. LM is responsive to the external (or host) voltages:

> Numeral 10 is a circuit for generating a limiter enable signal LM. If the external power supply voltage is higher than the internal power supply voltage, thereby operating the voltage converter circuit (voltage limiter), LM of a high voltage ("1") is generated whereas if the external power supply voltage is decreased to a value equal to the internal power supply voltage, LM of a low voltage of ("0") is generated. In the latter case, the external power supply voltage is directly applied to the main circuit block and also the voltage converter is not operated to restrain power consumption. In the example as shown, when the power supply voltage Vcc is compared with the reference voltage Vcx, and LM is generated if the former is larger than the latter. (Col 6, lines 23 – 36)

As such, there is no "... bypass enable signal operable *responsive to a signal generated by the host device indicating that the power up of the host is complete".* In *Etoh et al.*, a bypass controller LM is responsive to the external power supply (or host voltage) irrespective of any other signals – there is no separate "*signal generated by the host device indicating that the power up of the host is complete".*

Finally, the Examiner states that:

> a bypass enable signal (LM) [is] operable responsive to a signal (4) generated by the host device indicating that the power up of the host is complete (signal 4 is high when ExtVcc is above a predetermined Voltage

LM is not responsive to signal 4 nor is signal 4 a signal indicated a power up is complete.

Initially, it is noted that LM is not responsive to signal 4. LM is responsive to the external voltage only, as indicated above. Signal 4 is not coupled to a bypass element (SWa or SWc), but a Switch SW:

> In this power supply circuit, numeral 3 is a voltage drop detection circuit for the power supply voltage, SW is a switch for preventing current from flowing the battery to an external power supply terminal during data retention, numeral 4 is a control signal for the switch, B is a battery by which the entire LSI chip operates in the data retention mode (Vbt is its voltage), and D is a diode for preventing current from flowing the external

power supply into the battery in the normal operation mode. (Col. 4 line 65 – Col. 5 line 7)

To the extent the Examiner alleges that signal 4 operates switch SW and therefore the LM Gen Ckt operates responsive to the voltage there through, signal 4 still does not meet the limitation because it indicates nothing about whether the power up of the host is complete – signal 4 is responsive to the host voltage – whatever it's level. There is no indication of the state of pwer up of the host device provided by signal 4 (or any other signal in *Etoh et al.).*

Therefore, it is respectfully submitted claims 1, and claims 2-3, 5-15 dependent from claim 1 and including all the limitations thereof, are not anticipated by *Etoh et al.*.

Claims 16 – 17, 19, 20

For substantially the same reasons as set forth above, it is respectfully submitted claims 16 – 17, 19, 20 are not anticipated by *Etoh et al.*

Claim 16 includes limitations calling for:

providing a voltage regulator having a host voltage input and an output, and including a regulator bypass shorting *the host voltage* at the input to the output responsive to an enable signal;

setting the bypass to off prior to power up of a host device;

responsive to a power up completion signal from a host device, determining the power supplied by the host;

As noted with respect to claim 1, the elements of *Etoh et al.* do not provide a "power up completion" signal, but merely a V_{cc} voltage which is controlled to a memory device. There is no separate signal for power up completion of a host.

Moreover, there is no teaching of " ... setting the bypass to off prior to power up of a host device..." In the rejection, the Examiner cites no support for this element. Examination of the reference yields no disclosure of an equivalent step in combination with the other steps of this claim. Hence, two separate steps of claim 16 are wholly not disclosed in the reference.

It is therefore respectfully submitted claim 16, and claims 17, 19 - 20 dependent from claim 16 and including all the limitations thereof, are not anticipated by *Etoh et al.*.

Claims 25 - 36

For substantially the same reasons as set forth above, it is respectfully submitted claims 256 – 31 or 32 – 26 are not anticipated by *Etoh et al.*

Claim 25 includes limitations similar to those set for the above with respect to claim 1 and calls for:

> a bypass element coupled to selectively short *the host voltage at the input* to the output;
>
> a bypass control signal coupled to the bypass element and *responsive to a host system power up completed signal* which enables the bypass element when the host voltage is below a threshold level.

No such host system power up completed signal enabling a bypass element is disclosed. Hence, it is respectfully submitted claim 25 and claims 26 – 31 dependent there from are not anticipated by *Etoh et al.*

Claim 32 includes limitations similar to those set for the above with respect to claim 16 and calls for:

> setting the bypass to off prior to power up of a host device;
>
> responsive to a command signal from the host device, determining the power supplied by the host; and

No such command signal is from a host device is disclosed in *Etoh et al.* , nor is any step of "setting the bypass to off prior to power up" are provided . Hence, it is respectfully submitted claim 25 and claim 33 dependent from claim 32are not anticipated by *Etoh et al.*

Claims 34 includes limitations similar to those set for the above with respect to claim 1 and calls for:

> a controller;
>
> ...
>
> a voltage regulator having a shorting element between a host voltage input and an output, the shorting element being responsive to a bypass control signal, *the bypass control signal provided by the controller responsive to a host system power up complete signal*

which enables the shorting element when the host supply voltage provided by the host is below a threshold level.

No separate "controller" is taught in *Etoh et al.*, nor is a "...the bypass control signal provided by the controller responsive to a host system power up complete signal" In the instant claim, the limitation is specific as to the origin of the bypass control signal as "provided by the controller" Since no "controller" is disclosed in *Etoh et al.*, no such signal can be provided.

Hence, it is respectfully submitted claim 34 and claims 35 - 36 dependent from claim 34 are not anticipated by *Etoh et al.*

Claim 4 and 18

Claims 4 and 18 were rejected as obvious over *Etoh et al.* in view of *Hellums* (U. S. Patent No 5,362, 988. As understood, *Hellums* is cited for the proposition that the bypass can comprise a plurality of transistors. (The Examiner's reference to "transistor TOS" is not understood – no such transistor can be found in either reference. It is understood that the examiner is referring to the bypass, previously alleged to be SWa of *Etoh et al.)*

Claims 4 and 18 depend from claims 1 and 16 respectfully, and it is respectfully submitted one of average skill in the are would not be led by the teachings of Claims 4 and 18 were rejected as obvious over *Etoh et al.* to provide an apparatus of method wherein a bypass is enabled responsive to "...a signal generated by the host device indicating that the power up of the host is complete" In *Etoh et al.,* the control path is understood to be provided by the IO buffer:

> Numeral 7 is an input/output buffer circuit; numeral 11 is an input/output bus for transmitting/receiving control signals and data between ... The input/output buffer circuit 7, which also serves as a voltage level converting circuit, can transmit/receive the control signals and data even if the logic swing in the chip does not coincide with that in the outside

One of average skill would be required to modify the teachings of *Etoh et al.* to utilize a control signal from an external device via the IO buffer (7) to provide "... a signal generated by the host device indicating that the power up of the host is complete..." There are no teachings in *Etoh et al.* that such a control signal is required or desirable, nor to use the control signal to enable a bypass. Hence, three independent inventive changes are required in *Etoh et al.* in order to reach the invention of claim 4 or 18.

Thus, it is respectfully submitted claims 4 and 18 are not obvious.

Claims 21 – 24

Claims 21 - 24 were rejected as obvious over *Etoh et al.* However, it is respectfully submitted that claims 21 – 24 are not obvious over *Etoh et al.*

Claims 21 – 24 depend from claim 16. Claim 16 requires

> setting the bypass to off prior to power up of a host device;
> *responsive to a power up completion signal from a host device*, determining the power supplied by the host;

One of average skill would be required to modify the teachings of *Etoh et al.* to utilize a control signal from an external device via the IO buffer (7) to provide "... a power up completion signal from a host device ..." and be required to set the bypass off. There are no teachings in *Etoh et al.* that such a control signal is required or desirable, nor to use the control signal to enable a bypass, nor anything as to the state of the bypasses (SWa) during power up. Hence, three independent inventive changes are required in *Etoh et al.* in order to reach the invention of claim 21 - 24.

Thus, it is respectfully submitted claims 21 - 24 are not obvious.

Based on the above amendments and these remarks, reconsideration of claims 1 - 36 is respectfully requested.

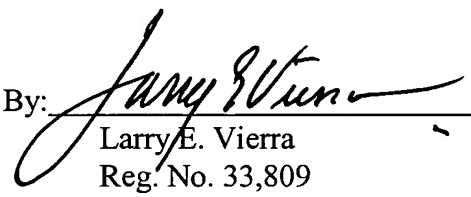
The Examiner's prompt attention to this matter is greatly appreciated. Should further questions remain, the Examiner is invited to contact the undersigned attorney by telephone.

Enclosed is a PETITION FOR EXTENSION OF TIME UNDER 37 C.F.R. § 1.136 for extending the time to respond up to and including today, September 12, 2005.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 501826 for any matter in connection with this response, including any fee for extension of time, which may be required.

Respectfully submitted,

Date: September 12, 2005

By: 

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